CLAIMS

What is claimed is:

1. An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache associated with a memory module, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments.

2. The apparatus of claim 1 wherein the segmentation of the cache lines is an optional feature.

3. The apparatus of claim 1, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

4. The apparatus of claim 3, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

5. The apparatus of claim 4, each of the plurality of arrays of tag address storage locations organized into 4 ways.

6. An apparatus, comprising:

a memory device; and

a data cache coupled to the memory device, the data cache controlled by commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments.

7. The apparatus of claim 6 wherein the segmentation of the cache lines is an optional feature.

8. The apparatus of claim 6, the data cache organized into a plurality of ways.

9. The apparatus of claim 8, the data cache organized into 4 ways.

10. A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller, the memory module including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, each tag address storage location in the array of tag address storage locations corresponding to a cache line divided into two segments.

11. The system of claim 10 wherein the segmentation of the cache lines is an optional feature.

12. The system of claim 10, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

13. The system of claim 12, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

14. The system of claim 13, each of the plurality of arrays of tag address storage locations organized into 4 ways.

15. The system of claim 14, a point-to-point interconnect to couple the memory controller to the memory module.